TENTATIVE TOSHIBA CMOS DIGITAL LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K11

DOT MATRIX LCD DRIVER

The T6K11 driver is designed for use in small to medium-sized dot matrix LCD panels. This driver can be interfaced to the MPU via a 4 / 8-bit (68 / 80-series) or a serial interface, and is operated asynchronously with the MPU. Since the T6K11 contains an RC circuit clock driver, it can generate the timing signals required for the LCD.
The display data can be stored in the built-in display RAM, whose cells each correspond to each dot on the dot-matrix LCD. The display data written to the RAM corresponds one for one to the LCD drive signals output by the device. Since the T6K11 has 160 outputs for the LCD drive (segment) signals that constitute display data and 65 outputs for the LCD drive (common) signals that constitute scanning signals, this single device allows you to drive an LCD panel comprised of up to 160 × 65 dots with a minimum of power requirement.

Unit : mm

T6K11	USER AREA PITCH	
	IN	OUT
(UBW, 5NS)	0.6	0.23

Please contact Toshiba or an authorized Toshiba dealer for the latest TCP specification and product lineup.
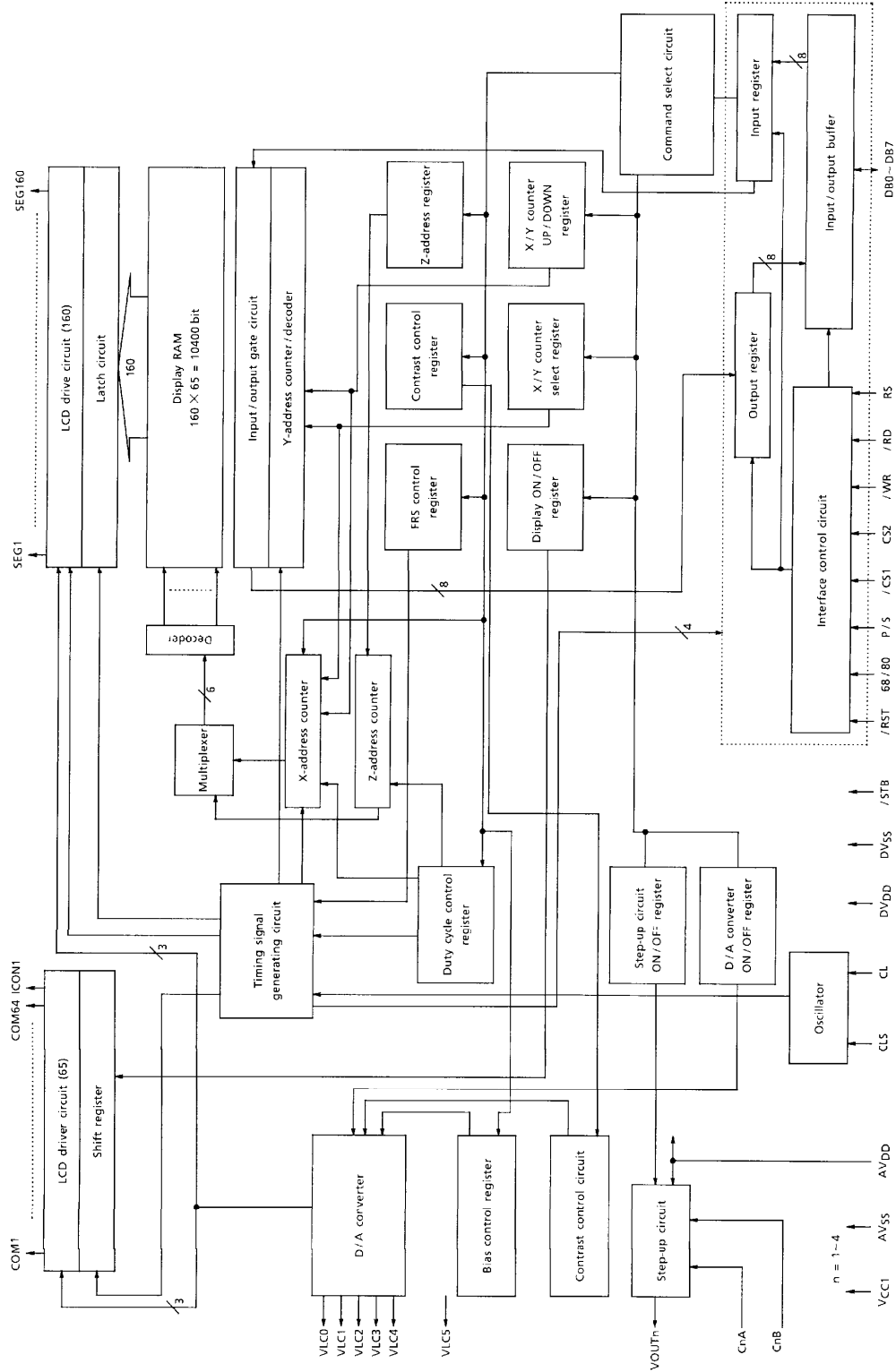
TCP (Tape Carrier Package)

To minimize its power consumption, the T6K11 has a display change mode (power save mode) in which only a 160 × 1-dot icon can be displayed. What's more, it has various built-in analog circuits such as a D / A converter for the LCD drive power supply, a step-up circuit (×2 to ×5), and a contrast control (electronic VR) circuit. All these circuits enable the LCD panel to be driven with a single power supply.

This product is under development; hence, specifications may change without notice. When you use this product, please refer to the latest technical datasheet.

FEATURES

- Display RAM : $160 \times (64 + 1) = 10{,}400$ bits

- LCD drive outputs : 160 segment outputs
  65 common outputs (including one common output for icon)

- RAM data direct display : Turned on when bit data in RAM = 1
  Turned off when bit data in RAM = 0

- Display duty cycle : 1 / 2 duty during power save mode
  1 / 35, 1 / 49, 1 / 57, or 1 / 65 duty during normal mode
  (Duty cycles in normal mode are set in software by the MPU.)

- Display modes : Normal mode .... Full display
  Power save mode ..... Icon display
  Standby mode .... Clock stop (all internal circuits turned off)

- MPU : 4 / 8-bit (68 / 80 series) parallel or serial interface

- Oscillator : Built-in RC oscillator (resistor and capacitor completely built-in), external
  clock input acceptable

- Power supply circuits : D / A converter for LCD drive power supply (temperature derating
  = 0.20% / °C), step-up circuit ($\times 2$ to $\times 5$), contrast control circuit

- Operating voltages : AV_{DD} (used for analog) = DV_{DD} to 5.5 V
  DV_{DD} (used for digital) = 1.8 to 3.3 V

- LCD drive voltage : V_{CC} = 16.5 V (max.)

- CMOS process

- Low power consumption : I_{SS} = 50 μA (Typ.) ..... Design target
  Conditions : AV_{DD} = DV_{DD} = 2.7 V, step-up circuit used ($\times 3$ mode), LCD
  nonloaded, Ta = 25°C, display data = all "checker pattern,"
  no data access from MPU

- Package : Bump chip (COG compatible)
  TCP (tape carrier package)

BLOCK DIAGRAM

T6K11-3

PIN ASSIGNMENT

Pin	Signal		Pin	Signal
45	COM32		44	VREG
46	COM31		43	OSCV$_{DD}$
47	COM30		42	PS
⋮	⋮		41	M68/80
75	COM2		40	V$_{LC5}$
76	COM1		39	V$_{LC4}$
77	ICON		38	V$_{LC3}$
78	SEG1		37	V$_{LC2}$
79	SEG2		36	V$_{LC1}$
			35	V$_{LC0}$
			34	V$_{CC}$
			33	V$_{OUT4}$
			32	C4B
			31	C4A
			30	V$_{OUT3}$
			29	C3B
			28	C3A
			27	V$_{OUT2}$
			26	C2B
			25	C2A
155	SEG78		24	V$_{OUT1}$
156	SEG79		23	C1B
157	SEG80		22	C1A
158	SEG81		21	AV$_{DD}$
159	SEG82		20	AV$_{SS}$
160	SEG83		19	CLS
			18	CL
			17	DV$_{SS}$
			16	DV$_{DD}$
			15	DB7
			14	DB6
			13	DB5
			12	DB4
			11	DB3
			10	DB2
226	SEG159		9	DB1
237	SEG160		8	DB0
238	COM33		7	/RD
239	COM34		6	/WR
			5	RS
			4	/RST
			3	CS2
			2	/CS1
268	COM63		1	/STB
269	COM64			
270	ICON			

T 6 K 1 1

(TOP VIEW)

(*) :   The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package.

PAD COORDINATES

(Note) : Please refer to the T6K11 technical datasheet for the pad layout and coordinates values.

PIN FUNCTION

PIN NAME	PIN No.	I / O	FUNCTION
SEG1~160		O	LCD drive segment signals
COM1~64		O	LCD drive common signals
ICON		O	LCD drive common signal (used for icon)
DB0~DB5		I / O	Data bus When P / S = low, DB0 to DB5 are placed in the high-impedance state.
DB6 (SCK)		I / O	Data bus When P / S = low, this bus functions as the serial interface's data synchronizing clock (SCK).
DB7 (SI)		I / O	Data bus When P / S = low, this bus functions as the serial interface's data input pin (SI).
RS		I	Register mode select signal ● When RS = low, this input is recognized as a register number. ● When RS = high, this input is recognized as the data to be written to the register.
/ RD (E)		I	Read select signal ● When 68 / 80 = low (80-series MPU selected), data is output while this pin is held low. Data is latched in at the active edge. ● When 68 / 80 = high (68-series MPU selected), this pin is used as an enable signal input pin (E).
/ WR (R / W)		I	Write select signal ● When 68 / 80 = low (80-series MPU selected), data is latched at the rising edge of / WR. ● When 68 / 80 = high (68-series MPU selected), data read is selected if R / W = high or data write is selected if R / W = low.
/ CS1		I	Chip select signal (1) Data / commands can be input or output while this signal is held low.
CS2		I	Chip select signal (2) Data / commands can be input or output while this signal is held high.
/ RST		I	Reset signal The device is reset when this signal is pulled low.
P / S		I	Parallel / serial interface select signal ● The parallel interface is selected when this signal is high. ● The serial interface is selected when this signal is low.
68 / 80		I	68 / 80-series parallel MPU select signal ● The 68-series parallel MPU is selected when this signal is high. ● The 80-series parallel MPU is selected when this signal is low.

PIN NAME	PIN No.	I/O	FUNCTION
CLS		I	RC oscillator circuit ON/OFF select signal • The internal RC oscillator is turned on when CLS is high. • The internal RC oscillator is turned off when CLS is low, allowing for an external clock input to be used. In this case, use the CL pin to supply the external clock and leave C_2 open.
CL		I/O	Display clock input pin • When CLS = high, this pin functions as the internal RC circuit's clock monitor pin. • When CLS = low, this pin is used to input an external clock to the device.
/STB		I	Standby signal The device is placed in standby state when /STB is low.
C1A, C1B		—	External capacitor connecting pin for ×2 step-up
VOUT1		—	×2 step-up voltage output pin
C2A, C2B		—	External capacitor connecting pin for ×3 step-up
VOUT2		—	×3 step-up voltage output pin
C3A, C3B		—	External capacitor connecting pin for ×4 step-up
VOUT3		—	×4 step-up voltage output pin
C4A, C4B		—	External capacitor connecting pin for ×5 step-up
VOUT4		—	×5 step-up voltage output pin
V_{CC}		—	LCD drive power supply pin (1)
VLC0~VLC5		—	LCD drive power supply pin (2)
AV_{DD}, AV_{SS}		—	Analog circuit power supply pin
DV_{DD}, DV_{SS}		—	Digital circuit power supply pin

FUNCTION EACH BLOCK

● MPU interface unit

Depending on whether the 68/80 input and P/S input pins are high or low, the T6K11 selects a 4/8-bit parallel or a serial interface, allowing for data to be transferred from the MPU.

P/S	68/80	INTERFACE TYPE	/CS1	CS2	RS	/WR	/RD	DB7	DB6	DB5~0
H	L	80-series MPU (/CS1)	/CS1	H	RS	/WR	/RD	DB7	DB6	DB5~0
		80-series MPU (CS2)	L	CS2	RS	/WR	/RD	DB7	DB6	DB5~0
	H	68-series MPU	L	H	RS	R/W	E	DB7	DB6	DB5~0
L	—	Serial	L	H	RS	H/L	H/L	SI	SCK	Hi-Z

(Note) : "H" denotes the V_{DD} level ; "L" denotes the V_{SS} level.

(a) For the 80-series MPU

80-series MPU		T6K11
A0	→	RS
/IORQ	→	/CS1 (CS2 = "H")
/WR	→	/WR
/RD	→	/RD
D0~7	↔	DB0~7
/RESET	→	/RST

Reset circuit

(b) For the 68-series MPU

68-series MPU		T6K11
A0	→	RS
E	→	E
R/W	→	R/W
D0~7	↔	DB0~7
/RESET	→	/RST (/CS1 = "L", CS2 = "H")

Reset circuit

(c) For serial interface

Serial		T6K11
RS	→	RS
SI	→	SI
SCL	→	SCK
/RESET	→	/RST (/CS1 = "L", CS2 = "H", P/S = "L")

Reset circuit
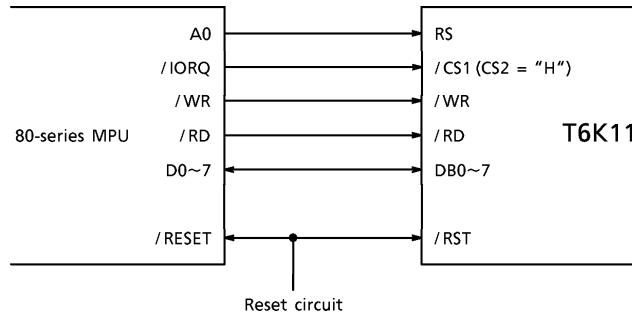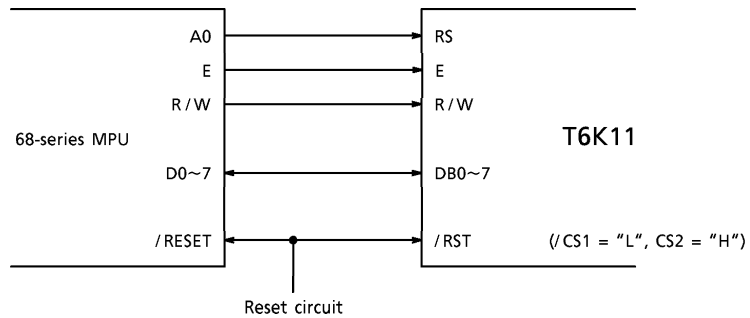
Fig.1

When the serial interface is selected (P / S = low), data and serial clock from the MPU are accepted providing that / CS1 = low and CS2 = high. The serial data input to the device is taken in from SI in order of DB7, DB6, ···DB0 at each rising edge of SCK, and are converted into parallel data at the 8th rising edge of SCK.
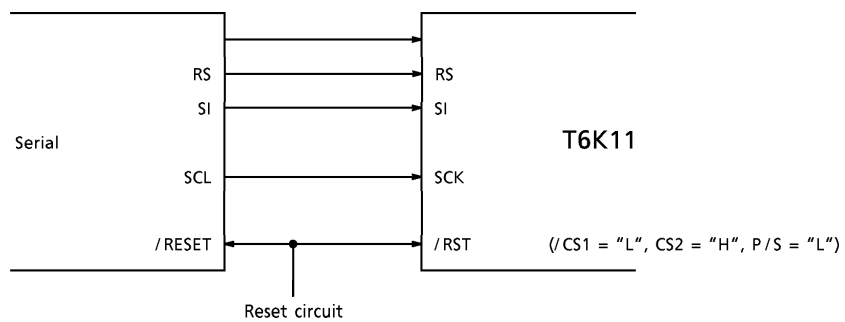
Recognition of the received data depends on the RS pin status at the 8th rising edge of SCK. If RS = low, the data is recognized as a register number set ; if RS = high, the data is recognized as write data. A serial interface timing chart is shown in Fig.2.

Note that when using the serial interface, the device can only write data to its internal logic and registers, and cannot read data and status.
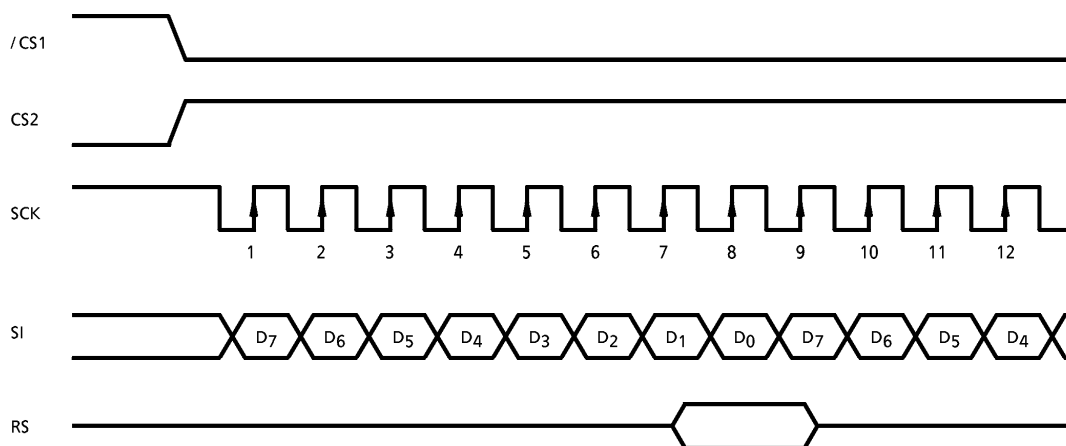
Fig.2

● Input / output buffer

This buffer is used to transfer data between the T6K11 and the MPU. For a parallel interface, this buffer is used as an 8-bit data bus ; for a serial interface, it is used to receive serial data and serial clock, with the serial data converted into parallel data before being taken into the internal circuit.

● Input register

This register holds the data from the MPU. The data held in this register is recognized as a register number or write data depending on whether RS is high or low.

● Output register

This register holds 8-bit data when transferring display RAM data or status information to the MPU.

● X-address counter

This counter is a 64-Up / Down counter used to hold the column address of the display RAM. When this counter is selected by a command, it is automatically incremented or decremented each time data is read or written to the display RAM.

● Y-address counter

This counter is a 20-Up / Down counter used to hold the row address of the display RAM. When this counter is selected by a command, it is automatically increased or decresed each time data is read or written to the display RAM.

● Z counter

This counter is a 64-Up counter used to supply the display data stored in the display RAM to the LCD drive circuit. The data held in the Z-address register is loaded into this counter as Z-address. Therefore, if this counter is set to 20, for example, it counts up from 20 to 21, 22, ⋯62, 63, (icon) and from 0 to 1, 2, ⋯18, 19, 20. The start line on the LCD screen is line 20 of the display RAM. Note, however, that the icon line (64) cannot be made the start line of the Z-address.

● X / Y counter up / down register

This register holds the data that selects the up-count or down-count mode for the X and Y counters.

● X / Y counter select register

This register holds the data that selects the X or Y counter to be used.

● Display ON / OFF register

This 1-bit register holds the data that determines whether the display be turned on or off. When turned OFF, outputs from the display RAM are reset. When turned ON, the display data corresponding to those in the display RAM are output to the LCD. Since the data in the display RAM does not affect display ON / OFF command control, the display RAM is not cleared anyway.

● Z-address register

This 6-bit register holds the data that determines the display start line. By setting Z-address in this register successively, it is possible to scroll the display up or down.

● Oscillator

The clocking source can be switched between the built-in RC oscillator or an external clock depending on the CLS pin status as shown in Fig.3. When CLS = high, the RC oscillator is enabled, supplying display clock to the internal logic. When CLS = low, the CL pin is switched for input, accepting an external clock.

Fig.3

● Timing signal generation circuit

This circuit generates the timing signals and operation clock required for display by dividing the clock frequency derived from the RC circuit or an external source.

● Shift registers

The T6K11 contains a 64-bit shift register necessary to shift the turn-on data required for the LCD drive common signals and a 1-bit shift register used for the icon.

● Duty cycle control register

This register holds the data that sets one of the four duty cycles that can be used.

● Contrast control register

This register holds 4-stage VLC control data and 64-stage contrast control data.

● Step-up circuit ON / OFF register

This register holds the data that determines whether the step-up circuit be turned on or off.

● D / A converter ON / OFF register

This register holds the data that determines whether the D / A converter be turned on or off.

● Bias control register

This register holds the data that sets one of the four bias values that can be used.

● Latch circuit

This circuit latches display data from the RAM.

● LCD drive circuit (segment)

The segment driver circuit consists of 160 drivers.
Each driver outputs one of the four LCD drive voltage levels depending on a combination of the display data from the latch circuit and the M signal (used for FR) as shown in Fig.4.
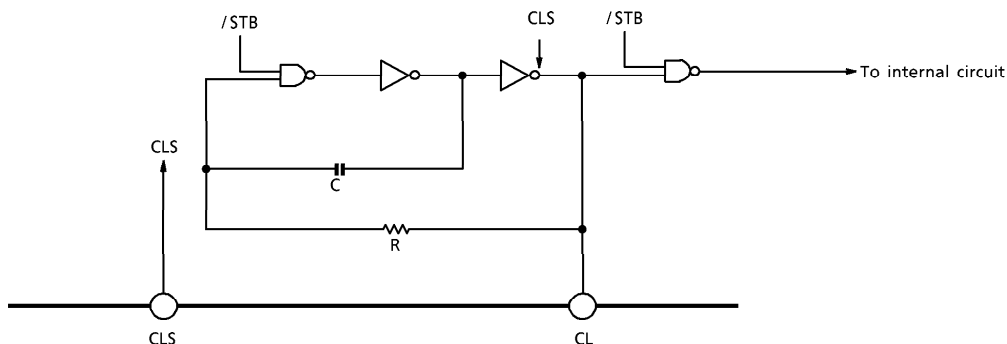The segment driver circuit is shown below.

Fig.4

● LCD drive circuit (common)

The common driver circuit consists of 65 drivers. Each driver outputs one of the four LCD drive voltage levels depending on a combination of the data from the shift register and the M signal (used for FR) as shown in Fig.5.
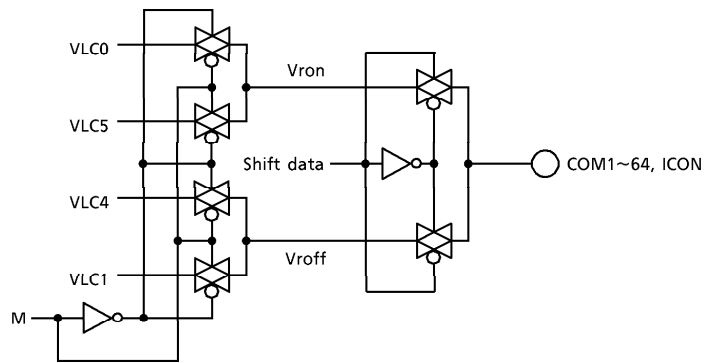The common driver circuit is shown below.

Fig.5

● Step-up circuit

The T6K11 contains a ×2/3/4/5 step-up circuit. When /RST = low or /STB = low, VOUT = 0 V (V_{SS} level). Normally, capacitors of more or less 2.2 μF are used for the step-up capacitor and step-up level retaining capacitor. Since the step-up circuit power supply AV_{DD} pin normally allows voltages to be input that are higher than possible for the digital-block power supply DV_{DD} pin, this circuit can generate the necessary LCD drive voltage. However, because the rated LCD drive voltage is 16.5 V (max.), care must be taken for the voltage condition (AV_{DD} voltage) used in step-up circuit and the number of boost steps to ensure that the boosted voltage (the voltage output from VOUT) will not exceed the rated voltage of 16.5 V.

(Note 1) : Relationship of power supply voltages

.... 5.5 V $\geqq$ AV_{DD} $\geqq$ DV_{DD} $\geqq$ 1.8 V

(Note 2) : Relationship between step-up output voltage and LCD drive voltage

.... 16.5 V $\geqq$ AV_{DD} × n ('n' denotes the number of boost steps.)
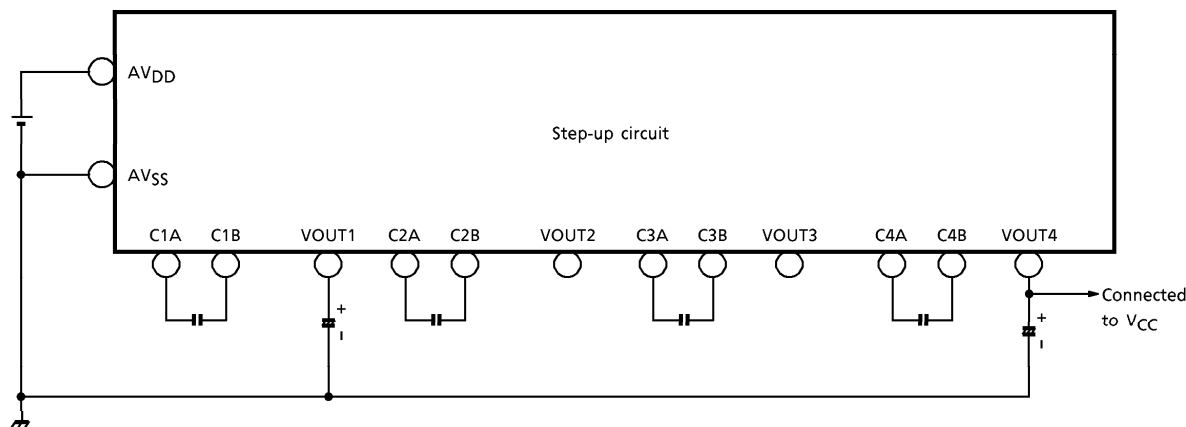
Example) : When using a ×5 step-up circuit

Fig.6

RECOMMENDED PIN PROCESSING WHEN USING A STEP-UP CIRCUIT

CONDITIONS	C1A, C1B	VOUT1	C2A, C2B	VOUT2	C3A, C3B	VOUT3	C4A, C4B	VOUT4
When using ×2 step-up circuit	Available	Available	Open	Open	Open	Open	Open	Open
When using ×3 step-up circuit	Available	Available	Available	Available	Open	Open	Open	Open
When using ×4 step-up circuit	Available	Available	Available	Open	Available	Available	Open	Open
When using ×5 step-up circuit	Available	Available	Available	Open	Available	Open	Available	Available

(Note) : "Available" means that a capacitor is connected to the pin.

● Contrast control, bias control, and D / A converter

The T6K11 contains a power supply generating circuit for LCD drive which is comprised of the D / A converter. The contrast (electronic VR) and bias required for each type of LCD panel are controlled by this circuit. Refer to Fig.7 for a block diagram of this power supply circuit.
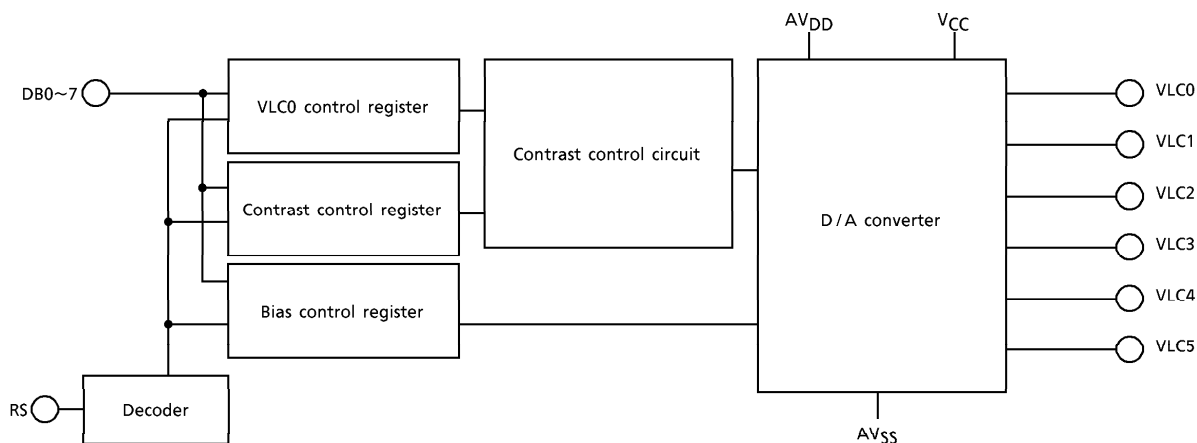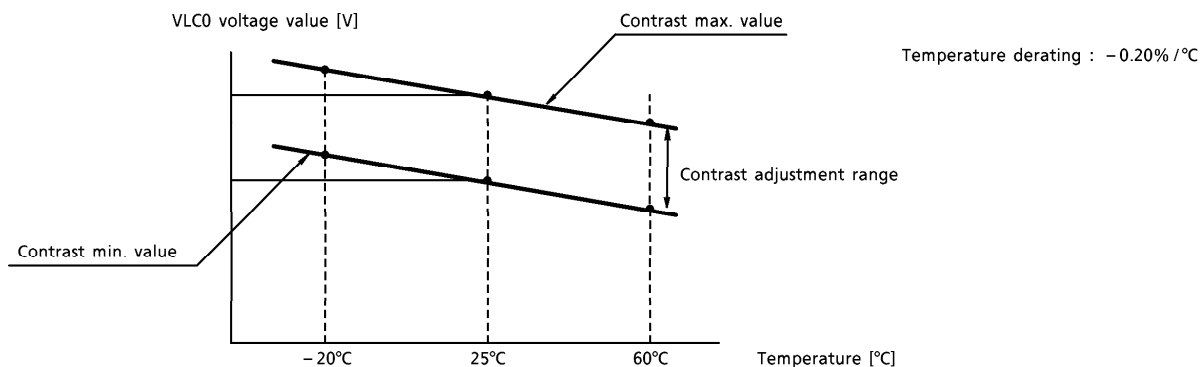

Fig.7

(Note) : The VLC0 voltage is derated with respect to temperature by − 0.20% / °C of centigrade in the range of minimum to maximum values. Therefore, voltage fluctuations due to temperature may be depicted like the one shown below.

RESISTOR RATIOS FOR ADJUSTING LCD DRIVE VOLTAGE (VLC0)

VLC0 CONTROL		VLC0 MAX CONTRAST (3FH)	VLC0 MIN CONTRAST (00H)	CONTRAST STEP VOLTAGE VALUE	V_{CC} INPUT VOLTAGE MIN VALUE	UNIT	REMARK
DB7	DB6						
0	0	(14.0)	(8.88)	(80 mV)	(15.5)	V	Ta = 25°C
0	1	(12.0)	(8.16)	(60 mV)	(13.5)	V	Ta = 25°C
1	0	(10.0)	(7.44)	(40 mV)	(11.5)	V	Ta = 25°C
1	1	(8.0)	(6.72)	(20 mV)	(9.5)	V	Ta = 25°C

VLC0 voltage value [V]

Contrast max. value

Temperature derating : −0.20% / °C

Contrast adjustment range

Contrast min. value

−20°C   25°C   60°C   Temperature [°C]

● About display RAM area

The T6K11's display RAM has a row of 160 cells in the segment direction and a row of 65 cells in the common direction, together constituting 10,400 bits of memory capacity. The relationship between the dot matrix LCD (= display screen) and the display RAM is such that one dot on the display screen corresponds to one bit in the display RAM as shown in Fig.8. If the data written to the display RAM is a logic 1, the corresponding dot on the display screen is turned on (black) ; if the data is a logic 0, the corresponding dot on the display screen is turned off (white). The relationship between display RAM and dot matrix LCD is shown below.
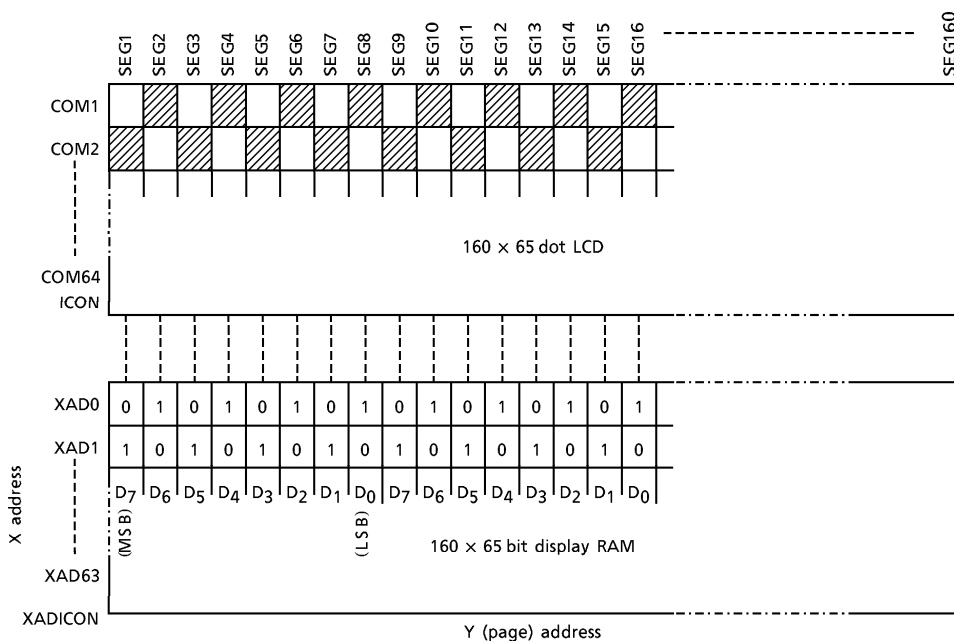

Fig.8

Note that if a duty cycle other than 1 / 64 is selected and a Z-address other than ZAD = 00h is set, the effective display RAM area is moved. The table below shows the relationship between duty cycle and Z-address settings and the resulting RAM area.

DUTY SETTING	EFFECTIVE RAM AREA		RANGE OF XAD WHEN Z-ADDRESS IS SET TO 00h	RANGE OF XAD WHEN Z-ADDRESS IS SET TO 05h	REMARK
	SEGMENT DIRECTION	COMMON DIRECTION			
1 / 35duty	160 lines	35 lines	XAD = C0~E1h, 80h	XAD = C5~E6h, 80h	
1 / 49duty	160 lines	49 lines	XAD = C0~EFh, 80h	XAD = C5~F4h, 80h	
1 / 55duty	160 lines	55 lines	XAD = C0~F5h, 80h	XAD = C5~FAh, 80h	
1 / 65duty	160 lines	65 lines	XAD = C0~FFh, 80h	XAD = C5~C4h, 80h	(Note 1)

(Note 1) : Even when ZAD is set to any value other than 00h, the effective display RAM area is the full size, so that the range of XAD is the same as XAD = C_0 to FFh and 80h shown above. Here, XADICON is expressed as 80h. For details about the specification of XADICON, refer to the command description (R_4) on page 20. The Z-address is effective in the range of XAD0 to 63 and does not affect XADICON.
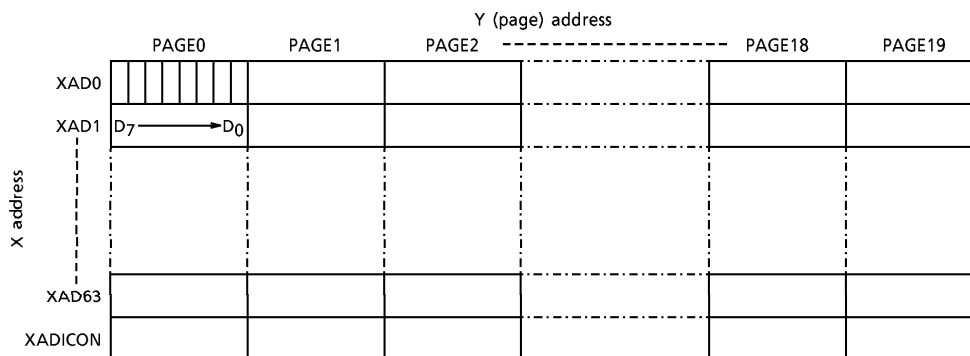
PAGE CONFIGURATION OF DISPLAY RAM

Fig.9

COMMAND DEFINITION

COMMAND	REG No.	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set Register (REG)	—	0	0	1	*	*	*	*	Register (0 to 15)			
Status Read (STRD)	—	0	1	0	*	*	*	*	RST	N/F	X/Y	U/D
Display Mode (DPE)	R_0	1	0	1	*	*	*	*	CDR	SDR	D/F	DP
Counter Mode (CSE)	R_1	1	0	1	*	*	*	*	*	*	X/Y	U/D
Analog Control Mode (APE)	R_2	1	0	1	CDA	DC	*	*	BIAS (0 to 3)		DUTY (0 to 3)	
Alternating Signal Mode (FRS)	R_3	1	0	1	*	*	FRS control (0 to 63)					
Set Y-address (SYE)	R_4	1	0	1	0	*	*	Y-address (0 to 19)				
Set X-address (SXE)		1	0	1	1	N/F	X-address (0 to 63)					
Set Z-address (SZE)	R_5	1	0	1	*	*	Z-address (0 to 63)					
Contrast Control (SCE)	R_6	1	0	1	VLC0 control	Contrast control (0 to 63)						
Data Write (DAWR)	R_7	1	0	1	Write data							
Data Read (DARD)		1	1	0	Read data							

Test Mode (TEST)	$R_{8\sim15}$	1	0	1	Test mode (Do not access these registers)

● Set register (REG)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	*	*	*	*	Register (0 to 15)			

This command selects a register No. When data is input after executing this command, the data is written to the register.

● R_0 : Display mode (DPE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	*	*	*	*	CDR	SDR	D/F	DP

This command sets a display mode. When data is input after executing this command, the contents shown below are set.

CDR : Sets the common data scanning direction.

CRD = 0 : Data is scanned in the direction ICON → COM64 → COM1.

CRD = 1 : Data is scanned in the direction COM1 → COM64 → ICON.

SDR : Sets the segment data direction.

SRD = 0 : SET1 → SEG128 with respect to the data direction DB7 → DB0

SRD = 1 : SET1 → SEG128 with respect to the data direction DB0 → DB7

D/F : Selects between normal display and icon display modes.

D/F = 0 : Icon display mode is selected.

D/F = 1 : Normal display mode is selected.

DP : Turns display ON or OFF.

DP = 0 : Display is turned OFF.

DP = 1 : Display is turned ON.

● R_1 : Counter mode (CSE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	*	*	*	*	*	*	Y/X	U/D

This command sets a counter mode. When data is input after executing this command, the contents shown below are set.

DB1	DB0	
0	0	Y-counter / Down mode is selected.
0	1	Y-counter / Up mode is selected.
1	0	X-counter / Down mode is selected.
1	1	X-counter / Up mode is selected.

The X and Y counters count the X and Y addresses of the display RAM when reading or writing to the RAM. This command selects either X or Y counter and also determines whether the selected counter counts up or down. Only one of the four available modes can be selected.

● R$_2$: Set analog control mode (APE)

RS	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	CDA	DC	*	*	BIAS (0 to 3)		DUTY (0 to 3)	

This command selects analog control and sets bias and duty cycle. When data is input after executing this command, the contents shown below are set.

CDA   : Turns the D / A converter for the LCD drive power supply ON or OFF.

CDA = 0 : The D / A converter is turned on.
CDA = 1 : The D / A converter is turned off.

DC   : Turns the step-up circuit on or off.

DC = 0 : The step-up circuit is turned on.
DC = 1 : The step-up circuit is turned off.

BIAS   : Sets a power supply bias for the LCD drive.

DB3	DB2	
0	0	Set to 1 / 6 bias.
0	1	Set to 1 / 7 bias.
1	0	Set to 1 / 8 bias.
1	1	Set to 1 / 9 bias.

DUTY : Sets a display duty cycle.

DB1	DB0	
0	0	Set to 1 / 35 duty.
0	1	Set to 1 / 49 duty.
1	0	Set to 1 / 57 duty.
1	1	Set to 1 / 65 duty.

● R$_3$: Set alternating signal mode (APE)

RS	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	*	*	FRS CONTROL (0 to 63)					

This command sets a number of lines at which the alternating signal (FR) should be inverted every time. When data is input after executing this command, the contents shown below are set.

FRS = 0 : A 1 / m (*1) duty is selected according to the DUTY that is set in the R$_2$ register and the alternating signal (FR) is inverted at a number of lines equal to the selected duty cycle.

FRS ≠ 0 : The alternating signal (FR) is inverted at a number of lines that equals the written data + 1.

(*1) : This is one of 1 / 35 duty, 1 / 49 duty, 1 / 57 duty, or 1 / 65 duty.

- R$_4$: Set Y-address (SYE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	0	*	*	Y-ADDRESS (0 to 19)				

This command sets a Y-address which is comprised of 20 pages. One of these pages is selected as data is written to the display RAM. When reset, the Y-address is set to page 0.

Set X-address (SXE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	1	N/F	X-ADDRESS (0 to 63)					

This command sets an X-address by selecting between display RAM and flag (icon) RAM. Address selection between display RAM and flag (icon) RAM is controlled by the data in DB7. When N/F = 1, the display RAM is selected. In this case, the low-order data (DB0 to DB5) are identified as X-address, and an X-address can be selected from addresses 0 through 63. When N/F = 0, the flag (icon) RAM address (64) is selected irrespective of the low-order data (DB0 to DB5). When reset, the X-address is set to address 0 in the display RAM.

- R$_5$: Set X-address (SZE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	*	*	Z-ADDRESS (0 to 63)					

This command sets a Z-address. The display RAM and flag (icon) RAM are separated and only the display RAM is selected. By selecting any address in the column direction of the display RAM, it is possible to set the first line on the LCD screen. The display data can be scrolled in the vertical direction by setting the first line in this way.
For example, if the Z-address is set to 20, the first line on the LCD screen corresponds to Z-address 20 in the display RAM, and the last line on the LCD screen corresponds to Z-address 19 in the display RAM. When reset, the Z-address is set to address 0.

- R$_6$: Contrast control (SCE)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	VLC0 CONTROL	CONTRAST CONTROL (0 to 63)						

This command sets VLC0 voltage adjustment resistance ratio and contrast control. These two controls adjust the density of display on the LCD screen. The density of display can be selected from 4 × 64 steps, where 00H is the lightest, and FFH the darkest. When reset, contrast control is set to 00H.

● R$_7$: Data write (DAWR) / data read (DARD)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	WRITE DATA							
1	1	0	READ DATA							

These commands enable data write and read to and from the display RAM. This single command register R$_7$ manages both data write and read to and from the display RAM. To write display data into the display RAM, set the X and Y addresses of the display RAM, then select this register (R$_7$) and write the data to the selected addresses of the display RAM. To read data from the display RAM, set the X and Y addresses of the display RAM, then select this register (R$_7$) and place it in the read mode (/RD = 0).

● R$_8$ to R$_{15}$: Test mode (TEST)

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	WRITE DATA							

These command registers are provided for test. Do not choose these registers.

FUNCTIONAL DESCRIPTION

● About the X-address and Y-address counters

The following explains the operation of the X-address and Y-address counters in connection with each command. A typical operation of the X-address counter is shown in Fig.9.
After a reset, the X-address (XAD) is set to 0 and the X-counter/Up mode is selected by the command CSE. Next, the X-address is set to 62 by the command SXE. Then when data is read or written to the display RAM, the X-address counter is automatically incremented as it continues counting up.
When data is read or written at XAD = 63, the X-address is recycled to 0. Now the X-address/ Down mode is selected by the command CSE. Then when data is read or written to the display RAM, the X-address counter is automatically decremented as it continues counting down. When data is read or written at XAD = 0, the X-address is recycled to 63.
The command CSE is effective for either X or Y counter selected. In the example here, the X-address counter is selected by CSE, so the Y-address counter does not count.
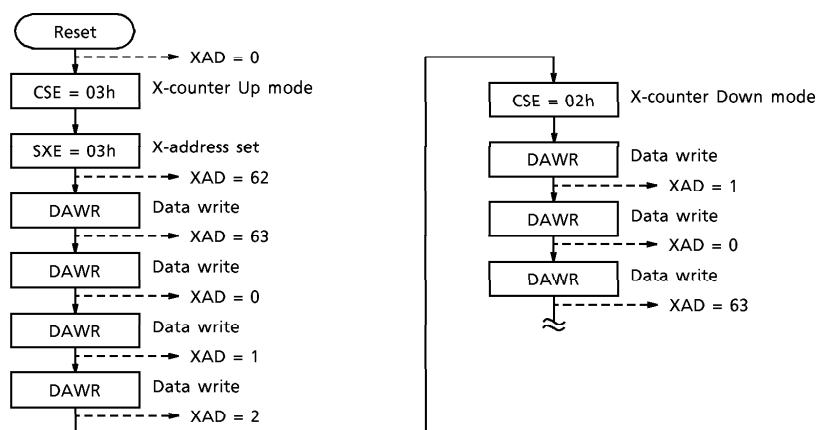

Fig.10

Fig.11 shows a typical operation of the Y (page)-address counter.

After a reset, the Y (page)-address (YAD) is set to 0 and the Y (page)-counter / Up mode is selected by the command CSE. Then when data is read or written to the display RAM, the Y (page)-address counter is incremented. When data is read or written at YAD = 19, the Y (page)-address is recycled to 0. Similarly, if the Y (page) Down mode is selected by the command CSE, the Y (page)-address is automatically decremented as the counter continues counting down. When data is read or written at YAD = 0, the Y (page)-address is recycled to 19. In the example here, the Y (page)-address counter is selected by CSE, so the X-address counter does not count.
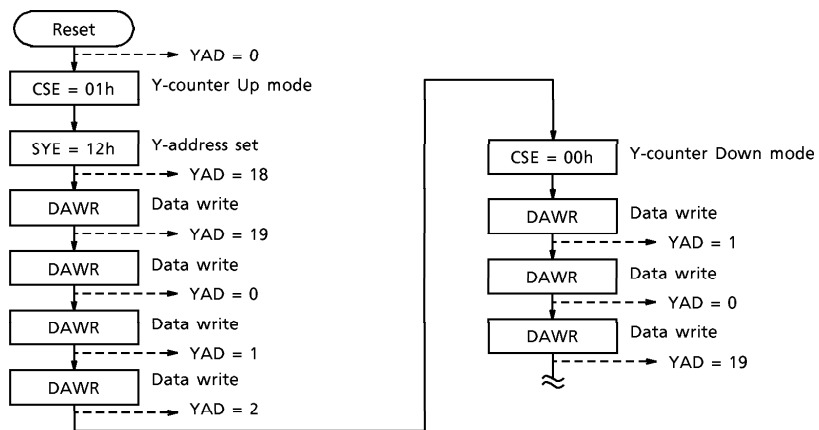

Fig.11

● Data read

When executing Data Read, the T6K11 directly accesses the display RAM addresses to read out data. Therefore, when the Data Read command is executed after setting the X and Y addresses, data is output immediately from the display RAM.
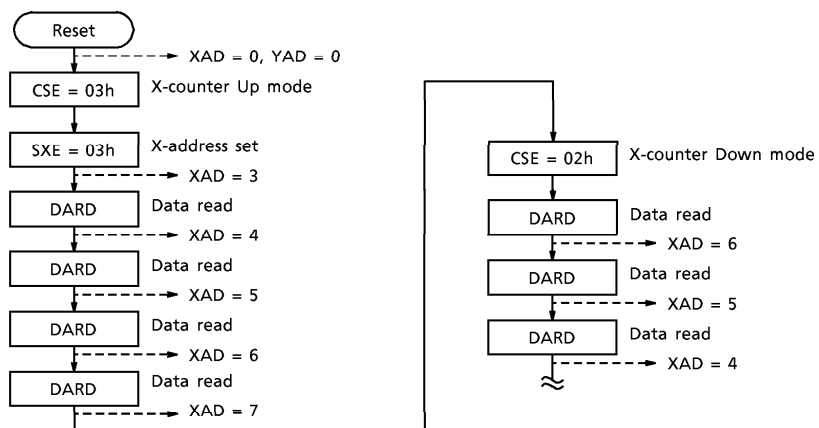

Fig.12

● FRS control

The T6K11 has a command FRS that allows you to choose a number of lines at which the alternating signal (FR) is inverted every time. The T6K11's alternating signal can be inverted in the range of two lines up to the same number of lines as the duty cycle. Normally, 00H may be selected for the FRS command, so that the FR signal is inverted when the same number of lines as the duty cycle are latched every time. To obtain better display quality, FRS need to be adjusted to match the characteristics of each type of LCD panel used.

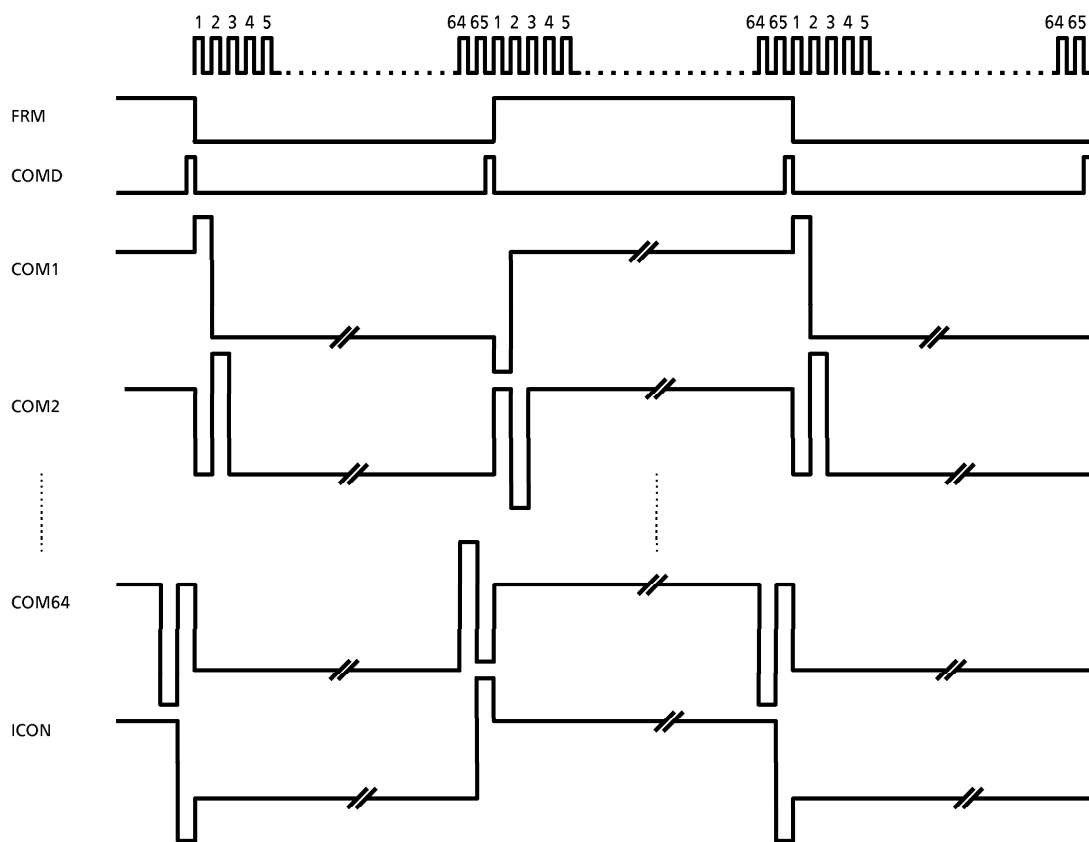(a) For 1 / 65 duty and FRS = 00H (inverted at 64 + 1 lines)

Fig.13

(b) For 1 / 35 and FRS = 10H (inverted at 16 + 1 lines)
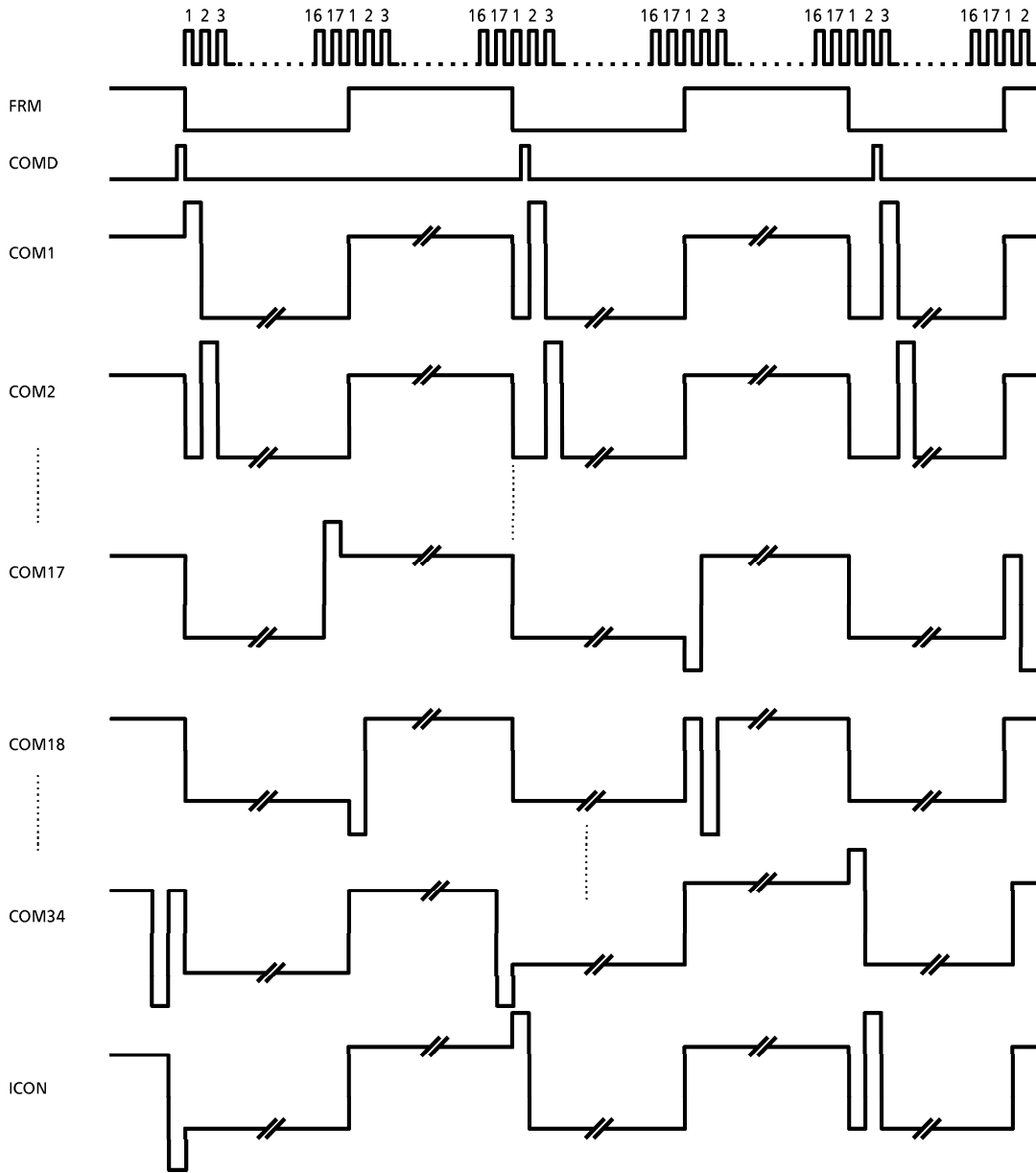

Fig.14

● Standby function

The T6K11 has a /STB pin. When input to this pin is pulled low, the T6K11 enters a standby state. In this state, the RC circuit clock driver is deactivated and the device is placed in a Low Power mode to suppress current consumption. Even when the T6K11 is in standby state (the RC circuit is deactivated, so is the LCD display clock), it can be communicated from the MPU. Since data read / write operations are possible while the display is turned off, this helps to reduce current consumption.

In standby state, all of the LCD drive power supply pins VLC0 to VLC5 are tied to the V_{SS} level. When the standby function is used, the data in the display RAM is the display data that has been stored in it before the standby function is turned on.

FUNCTION	OSCILLATOR	LCD DRIVE POWER SUPPLY	LCD DRIVE OUTPUT
Normal state	Operable	Operable	Operable
Standby state	Deactivated	Fixed to V_{SS} level	Fixed to V_{SS} level

● Reset function

The T6K11 has a /RST pin. When input to this pin is pulled low, the T6K11 is reset, with its internal circuits (register contents) initialized as shown below.

(1) Display direction .... CDR = 1, SDR = 1

(2) Display mode .... Normal display mode

(3) Display .... Turned OFF

(4) Counter .... Y-counter, Up mode

(5) Analog control .... CDA = 0, DC = 0

(6) Bias .... 1 / 9 bias

(7) Duty cycle .... 1 / 65 duty

(8) Alternating signal (FR) .... FRS = 00H
(FR inverted at the same number of lines as the duty cycle)

(9) Contrast .... 00H (lightest)

The T6K11 does not have a facility to reset the display RAM (to clear the data in it). In the initial state (immediately after power-ON), the display RAM contains indeterminate data which are either high or low. Therefore, Toshiba recommends using the Data Write command to execute a display clearing sequence before reading or writing to the display RAM.

● Oscillation frequency

The T6K11 contains an RC oscillator. The T6K11's frame frequency (f_{FR}) is derived from the RC circuit's oscillation frequency (f_{OSC}) by diving it an appropriate value. The relationship between the oscillation frequency (f_{OSC}) and the frame frequency (f_{FR}) is shown below.

DUTY CYCLE	FRS SELECTION	OSCILLATION FREQUENCY (f_{OSC})	CL FREQUENCY	f_{FR} FREQUENCY
1 / 65 duty	Inverted at duty	41 kHz	$\dfrac{f_{osc}}{8}$	$\dfrac{f_{osc}}{8 \times 65}$
1 / 57 duty	Inverted at duty	41 kHz	$\dfrac{f_{osc}}{10}$	$\dfrac{f_{osc}}{10 \times 57}$
1 / 49 duty	Inverted at duty	41 kHz	$\dfrac{f_{osc}}{12}$	$\dfrac{f_{osc}}{12 \times 49}$
1 / 35 duty	Inverted at duty	41 kHz	$\dfrac{f_{osc}}{16}$	$\dfrac{f_{osc}}{16 \times 35}$
1 / 65 duty	Inverted at 17 lines	41 kHz	$\dfrac{f_{osc}}{8}$	$\dfrac{f_{osc}}{8 \times 17}$
1 / 2 duty	Inverted at 2 lines	41 kHz	$\dfrac{f_{osc}}{256}$	$\dfrac{f_{osc}}{256 \times 2}$

(Note) : The T6K11 has its f_{FR} frequency varied by the FRS setup data. Therefore, consider the relationship between the duty cycle and the number of inversion lines when you adjust the f_{FR} frequency to suit the LCD panel used.

● LCD drive waveform

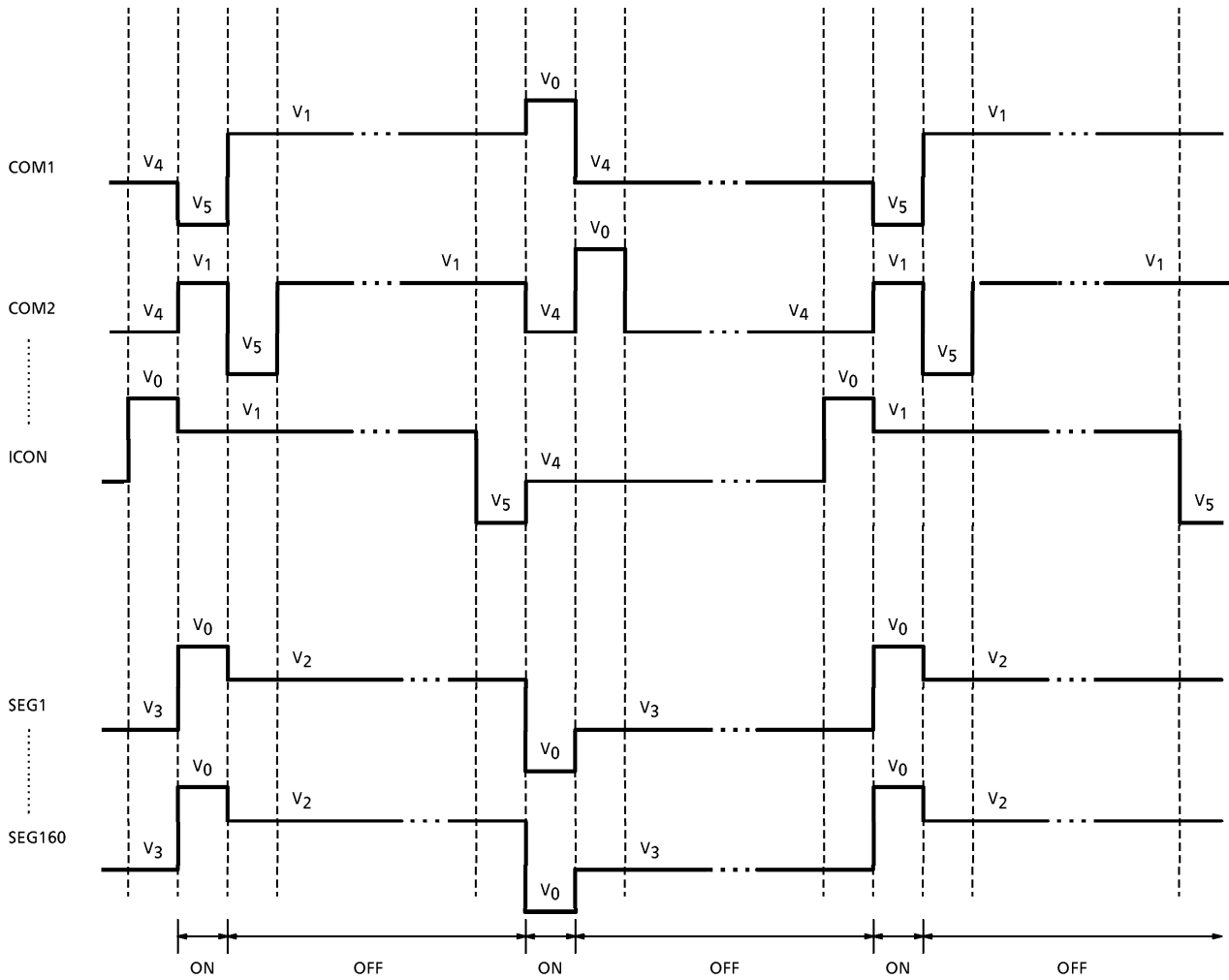(a) For normal display mode where duty cycle = 1 / 65 and FRS = 00h

Fig.15

(b) For power save mode where duty cycle = 1 / 2

MAXIMUM RATINGS (Referenced to V_{SS} = 0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTICS	SYMBOL	RATING	UNIT	REMARK
Power Supply Voltage (1)	DV_{DD}, AV_{DD}	$-0.3 \sim V_{SS} + 7.0$	V	(Note 1)
Power Supply Voltage (2)	(Note 2)	$-0.3 \sim V_{SS} + 18.0$	V	(Note 1), (Note 3)
Input Voltage (1)	V_{INA}	$-0.3 \sim AV_{DD} + 0.3$	V	(Note 1), (Note 4)
Input Voltage (2)	V_{IND}	$-0.3 \sim DV_{DD} + 0.3$	V	(Note 1), (Note 4)
Output Voltage (1)	V_{OA}	$-0.3 \sim V_{SS} + 18.0$	V	(Note 1)
Output Voltage (2)	V_{OD}	$-0.3 \sim DV_{DD} + 0.3$	V	(Note 1)
Operating Temperature	T_{opr}	$-25 \sim 75$	°C	—
Storage Temperature	T_{stg}	$-40 \sim 125$	°C	—

(Note 1) : These values are referenced to AV_{SS} = DV_{DD} = 0 V.
(Note 2) : V_{CC}, VLC0, VLC1, VLC2, VLC3, VLC4, VLC5
(Note 3) : The condition $V_{CC} \geqq$ VLC0 $\geqq$ VLC1 $\geqq$ VLC2 $\geqq$ VLC3 $\geqq$ VLC4 $\geqq$ VLC5 $\geqq$ must always be met.
(Note 4) : The condition $AV_{DD} \geqq DV_{DD}$ must always be met.
(Note 5) : If the device is used exceeding its absolute maximum ratings, the device may not only break down but also loose reliability and malfunction. Therefore, Toshiba recommends that for normal operation, the device be used within the range of electrical characteristics shown in the next page.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (1) referenced to DV_{DD} = 2.7 V, AV_{DD} = 2.7 V, VLC0 = 0 V, Ta = 25°C unless otherwise noted

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	RELEVANT PIN
Operating Voltage (1)		AV_{DD}	—	—	DV_{DD}	2.7	5.5	V	AV_{DD}
Operating Voltage (2)		DV_{DD}	—	—	1.8	2.7	3.3	V	DV_{DD}
Operating Voltage (3)		V_{CC} VCL0	—	—	6.0 − V_{SS}	—	16.5 − V_{SS}	V	V_{CC}, VCL0
Input Voltage	High Level	V_{IH}	—	—	$0.80 \times DV_{DD}$	—	DV_{DD}	V	(Note 1)
	Low Level	V_{IL}	—	—	0	—	$0.20 \times DV_{DD}$	V	
Output Voltage	High Level	V_{OH}	—	I_{OH} = 400μA	DV_{DD} − 0.2	—	DV_{DD}	V	DB0~DB7
	Low Level	V_{OL}	—	I_{OL} = 400μA	0	—	0.2	V	
Segment Driver ON-Resistance	Normal Mode	Rcol1	—	(Note 2)	—	—	7.5	kΩ	SEG1~SEG160
	Power Save Mode	Rcol2	—	(Note 3)	—	—	15.0	kΩ	
Common Driver ON-Resistance	Normal Mode	Rrow1	—	(Note 2)	—	—	1.5	kΩ	COM1~COM64 ICON
	Power Save Mode	Rrow2	—	(Note 3)	—	—	5.0	kΩ	
Input Leakage Current		I_{IL}	—	V_{IND} = DV_{DD}~GND	− 1	—	1	μA	(Note 1)
Output Leakage Current		I_{OL}	—	V_{OD} = DV_{DD}~GND	− 1	—	1	μA	DB0~DB7

(Note 1) : This applies to pins DB0 through DB7, RS, /WR, /RD, /CS1, CS2, /RST, /STB, P/S, 68/80, and CLS.

(Note 2) : Referenced to AV_{DD} = 2.7 V, DV_{DD} = 2.7 V, VLC0 = 11.0 V, V_{CC} = 16.5 V, 1/9 bias, current load Iload = 100 μA, Ta = 25°C.

(Note 3) : Referenced to AV_{DD} = 2.7 V, DV_{DD} = 2.7 V, VLC0 = 4.0 V, V_{CC} = 6.0 V, 1/12 bias, current load Iload = 100 μA, Ta = 25°C.

DC CHARACTERISTICS (2) referenced to DV_{DD} = 2.7 V, AV_{DD} = 2.7 V, VLC0 = 0 V, Ta = 25°C unless otherwise noted

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	RELEVANT PIN
Operating Frequency (Input Frequency)	CLIN	—	—	TBD	41	TBD	kHz	CL
Output Frequency	CLO	—	—	TBD	41	TBD	kHz	CL
External Clock Frequency	Fex	—	—	TBD	41	TBD	kHz	CL
External Clock Duty Cycle	Fduty	—	—	45	50	55	%	CL
External Clock Rise / Fall Time	Tr / Tf	—	—	—	—	10	ns	CL

DC CHARACTERISTICS (3) referenced to DV_{DD} = 2.7 V, AV_{DD} = 2.7 V, VLC0 = 0 V, Ta = 25°C unless otherwise noted

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	RELEVANT PIN
Output Voltage Characteristic (Using ×2 Step-up Circuit)	V_{O1}	(1)	(Note 4)	5.20	5.30	—	V	VOUT1
Output Voltage Characteristic (Using ×3 Step-up Circuit)	V_{O2}	(2)	(Note 5)	7.70	7.80	—	V	VOUT2
Output Voltage Characteristic (Using ×4 Step-up Circuit)	V_{O3}	(3)	(Note 6)	10.30	10.40	—	V	VOUT3
Output Voltage Characteristic (Using ×5 Step-up Circuit)	V_{O4}	(4)	(Note 7)	12.90	13.00	—	V	VOUT4

(Note 4) : Referenced to DV_{DD} = AV_{DD} = 2.7 V, Iload = 200 μA, V_{CC} = 5.40 V (supplied from external source), CnA-CnB = 1.0 μF, VOUTn-V_{SS} = 1.0 μF, CL = 41.0 kHz, Ta = 25°C.

(Note 5) : Referenced to DV_{DD} = AV_{DD} = 2.7 V, Iload = 200 μA, V_{CC} = 5.40 V (supplied from external source), CnA-CnB = 1.0 μF, VOUTn-V_{SS} = 1.0 μF, CL = 41.0 kHz, Ta = 25°C.

(Note 6) : Referenced to DV_{DD} = AV_{DD} = 2.7 V, Iload = 200 μA, V_{CC} = 5.40 V (supplied from external source), CnA-CnB = 1.0 μF, VOUTn-V_{SS} = 1.0 μF, CL = 41.0 kHz, Ta = 25°C.

(Note 7) : Referenced to DV_{DD} = AV_{DD} = 2.7 V, Iload = 200 μA, V_{CC} = 5.40 V (supplied from external source), CnA-CnB = 1.0 μF, VOUTn-V_{SS} = 1.0 μF, CL = 41.0 kHz, Ta = 25°C.

DC CHARACTERISTICS (4) referenced to DV_{DD} = 2.7 V, AV_{DD} = 2.7 V, VLC0 = 0 V, Ta = 25°C unless otherwise noted

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	RELEVANT PIN
Current Consumption (1)	ISS1	—	(Note 8)	—	85	TBD	μA	V_{SS}
Current Consumption (2)	ISS1	—	(Note 9)	—	95	TBD	μA	V_{SS}
Current Consumption (3)	ISS3	—	(Note 10)	—	250	TBD	μA	V_{SS}
Current Consumption (4)	ISS4	—	(Note 11)	—	20	TBD	μA	V_{SS}
Current Consumption (5)	ISS-STBO	—	(Note 12)	—	100	TBD	μA	V_{SS}
Current Consumption (6)	ISSSTB	—	(Note 13)	—	—	1	μA	V_{SS}

(Note 8) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = VOUT4 (using ×5 step-up), internal RC oscillator turned on (CL = 41 kHz), 1/9 bias, 1/65 duty, D/A converter turned on, LCD nonloaded, display pattern : all "white," no data access, normal display mode.

(Note 9) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = VOUT4 (using ×5 step-up), internal RC oscillator turned on (CL = 41 kHz), 1/9 bias, 1/65 duty, D/A converter turned on, LCD nonloaded, display pattern : "checker," no data access, normal display mode.

(Note 10) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = VOUT4 (using ×5 step-up), internal RC oscillator turned on (CL = 41 kHz), 1/9 bias, 1/65 duty, D/A converter turned on, LCD nonloaded, display pattern : "checker," data access performed (/CE = 1 MHz), normal display mode.

(Note 11) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = VOUT4 (using ×5 step-up), internal RC oscillator turned on (CL = 41 kHz), 1/12 bias, 1/2 duty, D/A converter turned on, LCD nonloaded, display pattern : "checker," no data access, power save mode.

(Note 12) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = 16.5 V, LCD nonloaded, data access performed (/CE = 1 MHz).

(Note 13) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, V_{CC} = 16.5 V, LCD nonloaded, no data access.

(*) : Current consumptions (1) through (6) are the design target values.

DC CHARACTERISTICS (5) referenced to DV_{DD} = 2.7 V, AV_{DD} = 2.7 V, VLC0 = 0 V, Ta = 25°C unless otherwise noted

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	RELEVANT PIN
D/A Converter Output Voltage Offset (1)	Vopoff1	—	(Note 14)	−150	—	150	mV	(Note 17)
D/A Converter Output Voltage Offset (2)	Vopoff2	—	(Note 15)	−150	—	150	mV	(Note 17)
D/A Converter Output Voltage Offset (3)	Vopoffs	—	(Note 16)	−100	—	100	mV	(Note 17)

(Note 14) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, 1/65 duty, 1/9 bias, V_{CC} = 15.0 V (supplied from external source), contrast control = Max., D/A converter : ON, step-up circuit : OFF, LCD nonloaded, normal display mode.

    VLC0 pin : 15.0 − VLC0 = Vopoff1
     VLC1 pin : (15.0 ÷ 8/9) − VLC1 = Vopoff1
     VLC2 pin : (15.0 ÷ 7/9) − VLC2 = Vopoff1
     VLC3 pin : (15.0 ÷ 2/9) − VLC3 = Vopoff1
     VLC4 pin : (15.0 ÷ 1/9) − VLC4 = Vopoff1

(Note 15) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, 1/2 duty, 1/12 bias, V_{CC} = 6.0 V (supplied from external source), contrast control = Max., D/A converter : ON, step-up circuit : OFF, LCD nonloaded, power save mode.

    VLC0 pin : 6.0 − VLC0 = Vopoff2
     VLC1 pin : (6.0 ÷ 8/12) − VLC1 = Vopoff2
     VLC2 pin : (6.0 ÷ 7/12) − VLC2 = Vopoff2
     VLC3 pin : (6.0 ÷ 2/12) − VLC3 = Vopoff2
   VLC4 pin : (6.0 ÷ 1/12) − VLC4 = Vopoff2

(Note 16) : Referenced to AV_{DD} = DV_{DD} = 2.7 V, AV_{SS} = DV_{SS} = 0 V, 1/65 duty, 1/9 bias, V_{CC} = 15.0 V (supplied from external source), contrast control = Max., D/A converter : ON, step-up circuit : OFF, LCD nonloaded, normal display mode.
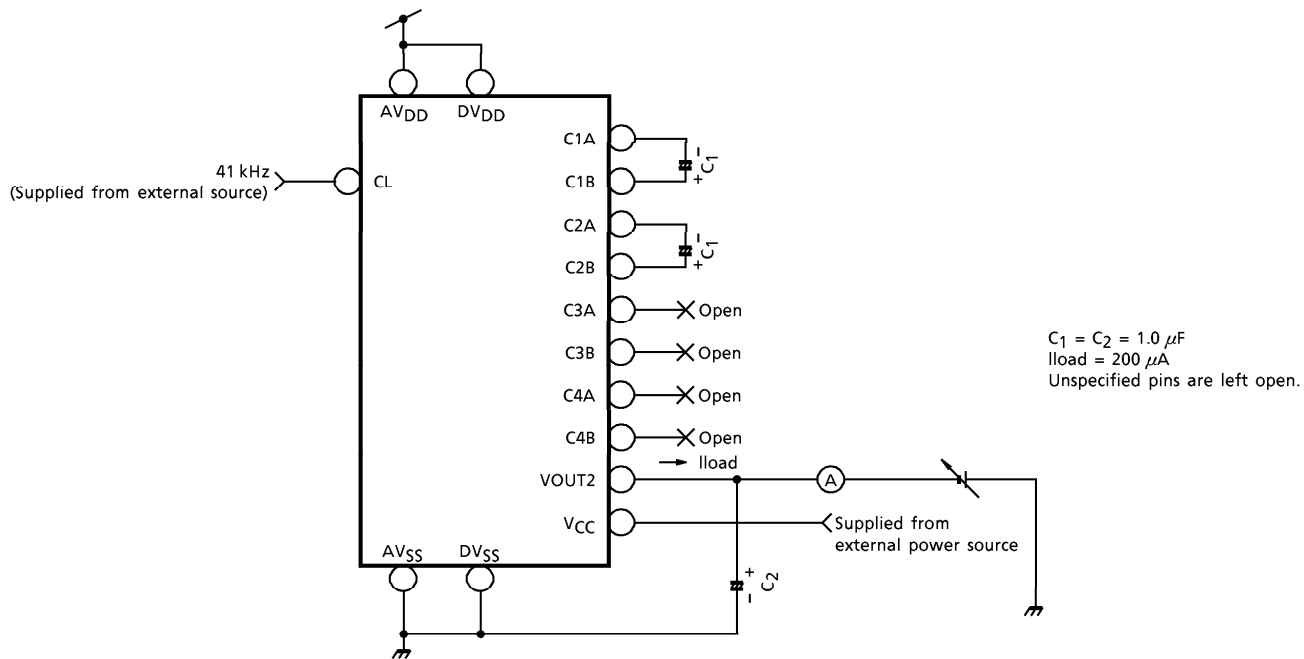   Vopoffs = ((VLC1 − VLC2) − (VLC0 − VLC1)) + ((VLC3 − VLC4) − (VLC4 − VLC5))

(Note 17) : This applies to pins VLC0, VLC1, VLC2, VLC3, VLC4, and VLC5.

TEST CIRCUITS

(1) Test circuit for cases when ×2 step-up circuit is used

$C_1 = C_2 = 1.0 \mu F$
Iload = 200 μA
Unspecified pins are left open.
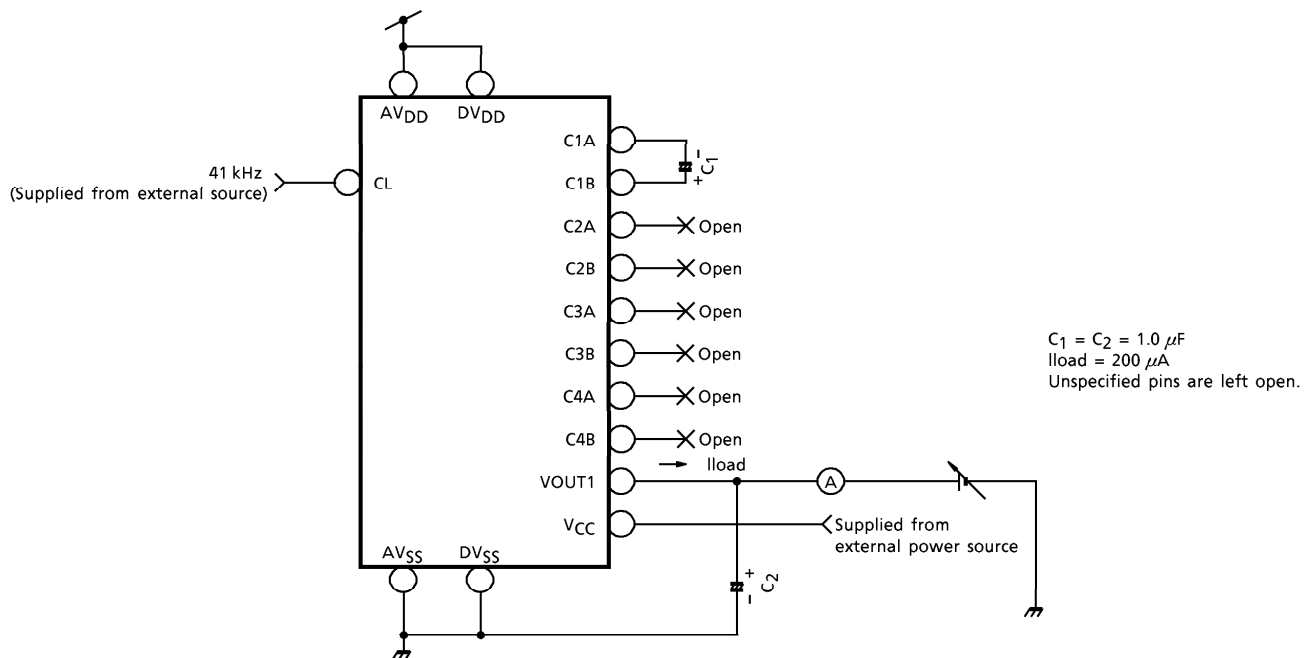
(2) Test circuit for cases when ×3 step-up circuit is used

$C_1 = C_2 = 1.0 \mu F$
Iload = 200 μA
Unspecified pins are left open.

(3) Test circuit for cases when ×4 step-up circuit is used

$C_1 = C_2 = 1.0 \, \mu F$
Iload = 200 μA
Unspecified pins are left open.

(4) Test circuit for cases when ×5 step-up circuit is used

$C_1 = C_2 = 1.0 \, \mu F$
Iload = 200 μA
Unspecified pins are left open.
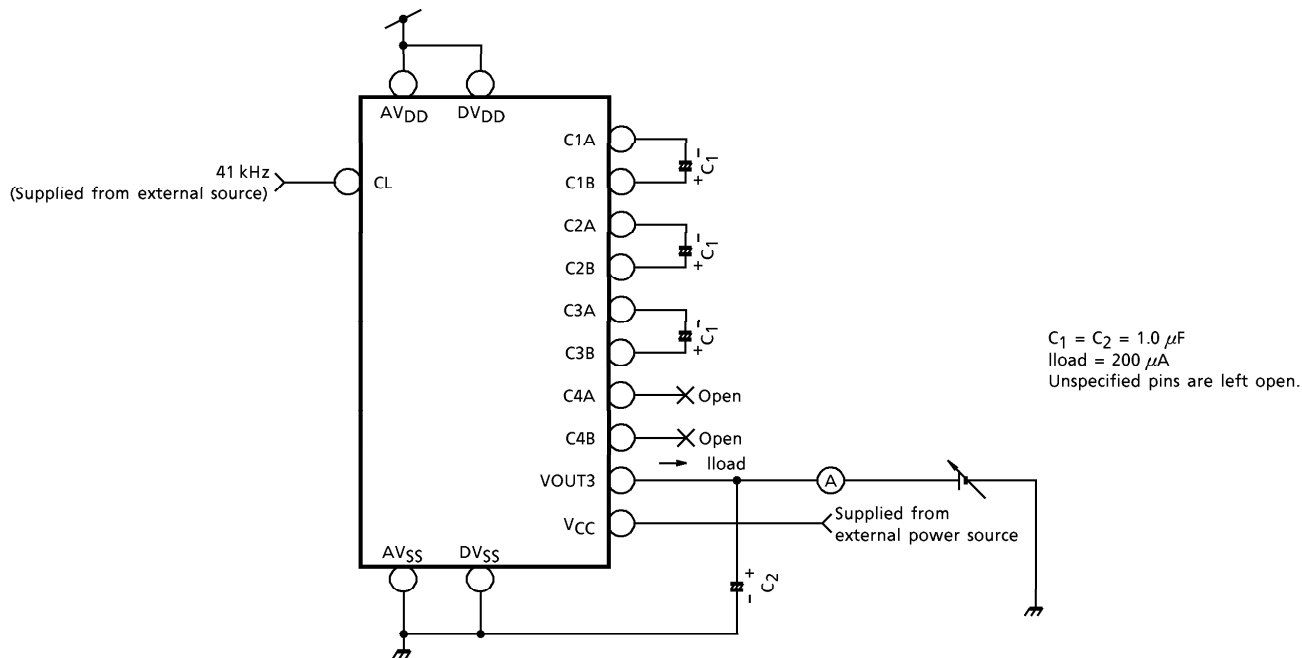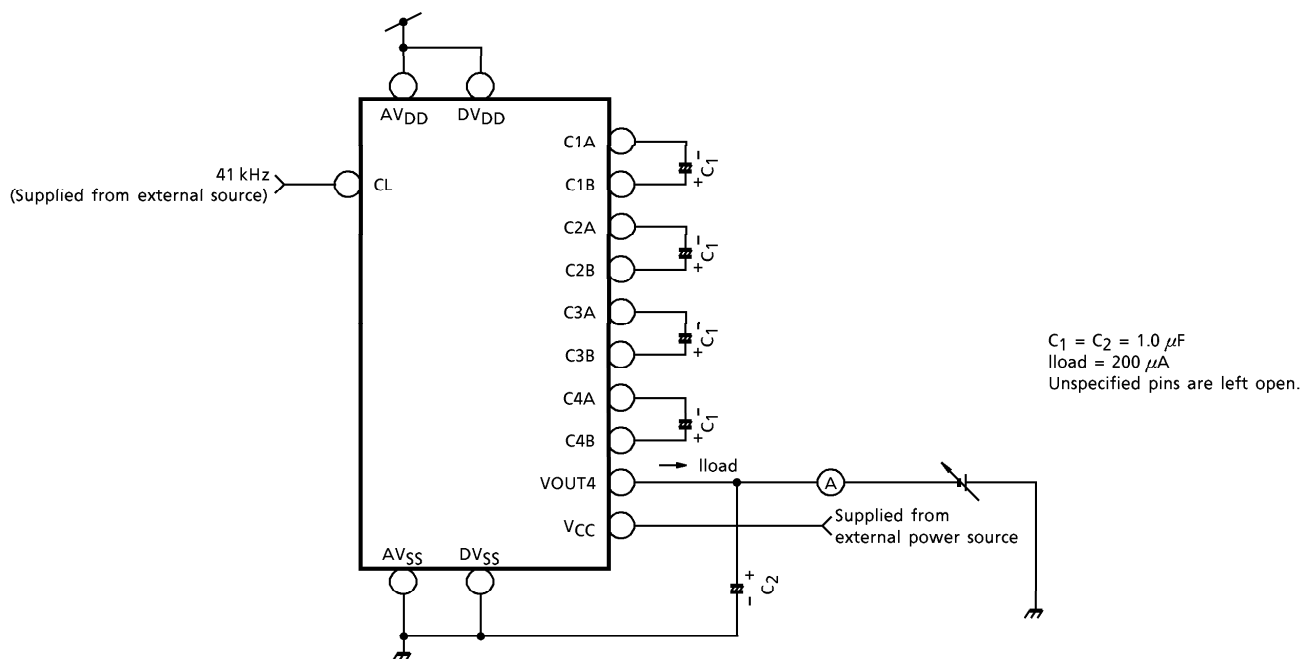
AC CHARACTERISTICS (1)

● 80-series parallel interface read / write characteristics

TEST CONDITION

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\,V,\ V_{DD} = 1.8 \text{ to } 2.7\,V,\ VLCD = 0\,V, \\ Ta = -20 \text{ to } 60°C \text{ unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	t_{cycE}	1000	—	ns
Enable Pulse Width	PWEL	500	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Setup Time	t_{AS}	25	—	ns
Address Hold Time	t_{AH}	25	—	ns
Data Setup Time	t_{DS}	80	—	ns
Write Data Hold Time	t_{DHW}	70	—	ns
Data Delay Time	t_{DD}	—	400	ns
Read Data Hold Time	t_{DHR}	50	—	ns

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\,V,\ V_{DD} = 2.7 \text{ to } 3.3\,V,\ VLCD = 0\,V, \\ Ta = -20 \text{ to } 60°C \text{ unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEL	300	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	15	ns
Address Setup Time	t_{AS}	20	—	ns
Address Hold Time	t_{AH}	20	—	ns
Data Setup Time	t_{DS}	60	—	ns
Write Data Hold Time	t_{DHW}	50	—	ns
Data Delay Time	t_{DD}	—	200	ns
Read Data Hold Time	t_{DHR}	20	—	ns

AC CHARACTERISTICS (2)

● 68-series parallel interface read / write characteristics

(*) /CS1 = L, CS2 = H

TEST CONDITION

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\,V,\ V_{DD} = 1.8 \text{ to } 2.7\,V,\ VLCD = 0\,V,\\ Ta = -20 \text{ to } 60°C \text{ unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	t_{cycE}	1000	—	ns
Enable Pulse Width	PWEL	500	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Setup Time	t_{AS}	25	—	ns
Address Hold Time	t_{AH}	25	—	ns
Data Setup Time	t_{DS}	80	—	ns
Write Data Hold Time	t_{DHW}	70	—	ns
Data Delay Time	t_{DD}	—	400	ns
Read Data Hold Time	t_{DHR}	50	—	ns

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\,V,\ V_{DD} = 2.7 \text{ to } 3.3\,V,\ VLCD = 0\,V,\\ Ta = -20 \text{ to } 60°C \text{ unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEL	300	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	15	ns
Address Setup Time	t_{AS}	20	—	ns
Address Hold Time	t_{AH}	20	—	ns
Data Setup Time	t_{DS}	60	—	ns
Write Data Hold Time	t_{DHW}	50	—	ns
Data Delay Time	t_{DD}	—	200	ns
Read Data Hold Time	t_{DHR}	20	—	ns

AC CHARACTERISTICS (3)

● Serial interface read / write characteristics
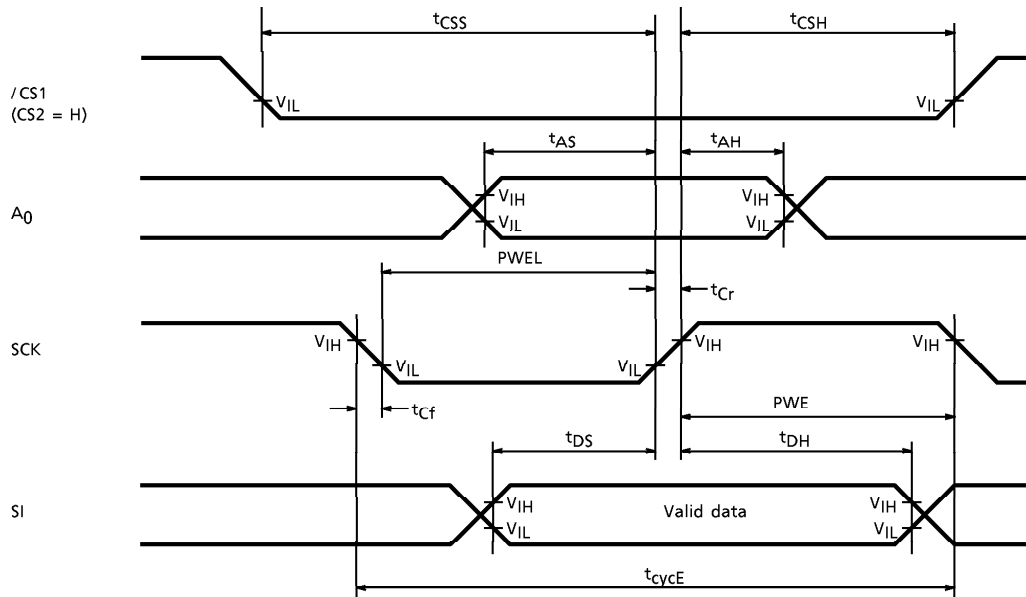
TEST CONDITION

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\text{ V, } V_{DD} = 1.8 \text{ to } 2.7\text{ V, VLCD} = 0\text{ V,}\\ \text{Ta} = -20 \text{ to } 60°\text{C unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Clock Cycle Time	t_{cycC}	1000	—	ns
Clock Pulse Width	PWCL, PWCH	500	—	ns
Clock Rise / Fall Time	t_{Cr}, t_{Cf}	—	20	ns
CS Setup Time	t_{CSS}	300	—	ns
CS Hold Time	t_{CSH}	300	—	ns
Address Setup Time	t_{AS}	300	—	ns
Address Hold Time	t_{AH}	300	—	ns
Data Setup Time	t_{DS}	—	250	ns
Data Hold Time	t_{DH}	250	—	ns

$\left(\begin{array}{l}\text{Referenced to } V_{SS} = 0\text{ V, } V_{DD} = 2.7 \text{ to } 3.3\text{ V, VLCD} = 0\text{ V,}\\ \text{Ta} = -20 \text{ to } 60°\text{C unless otherwise noted}\end{array}\right)$

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Clock Cycle Time	t_{cycC}	400	—	ns
Clock Pulse Width	PWCL, PWCH	150	—	ns
Clock Rise / Fall Time	t_{Cr}, t_{Cf}	—	15	ns
CS Setup Time	t_{CSS}	250	—	ns
CS Hold Time	t_{CSH}	250	—	ns
Address Setup Time	t_{AS}	250	—	ns
Address Hold Time	t_{AH}	250	—	ns
Data Setup Time	t_{DS}	—	150	ns
Data Hold Time	t_{DH}	150	—	ns

EXAMPLE OF APPLICATION CIRCUIT

T6K11

- Internal RC oscillator used

- ×5 step-up circuit used

- 8-bit parallel MPU interface used